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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,162	12/15/2003	Ji Yong Park	0091.1031	2087

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STEIN MCEWEN, LLP
1400 EYE STREET, NW
SUITE 300
WASHINGTON, DC 20005

EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,162	PARK ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to RCE filed April 14, 2009.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "offset region" recited in claims 1 and 7 must be shown or the feature canceled from the claims, because only LDD regions are shown in Figs. 5 and 6. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 12 is objected to because of the following informalities: on line 3, "light" should be replaced by "lightly". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 3-5, 7 and 9-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Regarding claims 1 and 7, Applicants originally disclosed that "the width between "primary" crystal grain boundaries of polysilicon forming the activation layer 13 should be wider than that of the LDD region II" ([0036] of current Application), and originally claimed that "a width of an activation layer including the LDD region or offset region is shorter than a distance between the primary crystal grain boundaries" in original claims 2 and 8. However, Applicants did not originally disclose that "a width of the offset region, included in an activation layer, is smaller than a distance between the primary crystal grain boundaries (emphasis added)" as recited in amended claims 1 and 7. Claims 3-5 depend on claim

1, and claims 9-11 depend on claim 7, and therefore claims 3-5 and 9-11 also fail to comply with the written description requirement.

5. Claims 5 and 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding claims 5 and 11, the limitation “the primary crystal grain boundaries are perpendicular to a current direction” is not enabling, because even though Applicants used straight lines to show “primary” crystal grain boundaries in Fig. 6 of current Application, actual “primary” grain boundaries cannot be formed in straight lines, and therefore non-straight lines cannot be perpendicular to a current direction.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 3-5, 7 and 9-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 1 and 7, it is not clear whether Applicants claim "an offset region having no doping", or an offset region not intentionally doped or lightly doped. Even though Applicants disclosed that "an offset region refers to a region that is not doped” in paragraph [0028] of current Application, a polysilicon layer formed from an amorphous silicon would *inherently* comprise impurities or dopants incorporated during a solidification process or from

diffusion of dopants from nearby source and drain regions. Claims 3-5 depend on claim 1, and claims 9-11 depend on claim 7, and therefore claims 3-5 and 9-11 are also indefinite. In the below prior art rejections, it is interpreted that the "offset region" is not intentionally doped but still is doped at a low doping concentration or lightly doped.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 3-7 and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Oka et al. (US 6,184,541).

Regarding claims 1, 4, 5, 7, 10 and 11, Oka et al. disclose (a flat panel display device (col. 2, lines 27-29) comprising) a thin film transistor (TFT) (Figs. 1a and 1b) comprising an offset region (region between rightmost primary grain boundary in channel region 8 and region 4, or portion of region 4 included in width "d" on the right side) (no doping is disclosed for channel region 8, and col. 3, lines 60-66 and col. 4, lines 63-66) having no doping and a plurality of primary crystal grain boundaries (2) (boundaries substantially perpendicular to current direction) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are not positioned in the offset region, and wherein a width of the offset region (region between rightmost primary grain boundary in

channel region 8 and region 4, or portion of region 4 included in width "d" on the right side), included in an activation layer (composite layer of 6, 7 and 8) (col. 3, lines 42-43), is smaller than a distance between the primary crystal grain boundaries (2) (for example, a distance between two primary crystal grain boundaries wherein one primary crystal grain boundary is selected from each region 5) (claims 1 and 7), wherein the thin film transistor may be used in an LCD device (col. 2, lines 27-29) (claims 4 and 10), and the primary crystal grain boundaries (2) are perpendicular to a current direction between source and drain regions (6 and 7, respectively) of the thin film transistor (claims 5 and 11).

Regarding claims 3 and 9, the limitation "the polysilicon substrate is formed by a sequential lateral solidification (SLS)" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Regarding claim 6, Oka et al. disclose a thin film transistor (TFT) (Figs. 1a and 1b) comprising a lightly doped drain (LDD) region or offset region (portion of region 4 included in width "d" on the right side) (col. 3, lines 60-66, and col. 4, lines 63-66) and a plurality of primary crystal grain boundaries (2) (boundaries substantially perpendicular to current direction) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are

positioned in channel, source and drain regions (8 and two regions denoted as 5) (col. 3, lines 42 and 39-40) but not positioned in the LDD or offset region (portion of region 4 included in width "d" on the right side), and wherein a width (d) of the LDD region or offset region is less than a distance between two adjoining primary crystal grain boundaries (one rightmost primary grain boundary in channel region 8 and another leftmost primary grain boundary in region 4 on the right) as clearly shown in Fig. 1(a).

Regarding claim 12, Oka et al. disclose a flat panel display device (col. 2, lines 27-29) comprising a thin film transistor (Figs. 1a and 1b) comprising a lightly doped drain (LDD) region or offset region (portion of region 4 included in width "d" on the right side) (col. 3, lines 60-66, and col. 4, lines 63-66), and a plurality of primary crystal grain boundaries (2) (boundaries substantially perpendicular to current direction) (col. 3, lines 36-37), wherein the thin film transistor (Figs. 1a and 1b) is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are positioned in channel, source and drain regions (8 and two regions denoted as 5) (col. 3, lines 42 and 39-40) but not positioned in the LDD or offset region (portion of region 4 included in width "d" on the right side), and wherein a width (d) of the LDD region or offset region is less than a distance between two adjoining primary crystal grain boundaries (one rightmost primary grain boundary in channel region 8 and another leftmost primary grain boundary in region 4 on the right) as clearly shown in Fig. 1(a).

Response to Arguments

10. Applicants' arguments with respect to claims 1, 6, 7 and 12 have been considered but are moot in view of the new grounds of rejection.

Applicants argue that “furthermore, Applicants respectfully note that region "d" is not an LDD region as noted in the Office Action, but is rather part of the LDD region "D.", that “therefore, the LDD region is "D" and not "d" (see column 3, lines 36-50), as suggested in the Office Action”, and that “therefore, the primary crystal grain boundary 2 is positioned in the LDD region since the distance between the primary crystal grain boundaries is smaller than D (see Fig. 1(b))”. Merriam-Webster dictionary defines “region” as “an often indefinitely defined part or area”, and therefore unless Applicants claim a specific structure of the LDD region, a portion of 4 of width "d" may be referred to as an LDD region, especially when Oka et al. refer to "d" as “an effective length” of the low concentration region (col. 3, lines 65-66), which suggests that the portion of region 4 included in width "d" is an effective low concentration region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
June 30, 2009
/Kenneth A Parker/
Supervisory Patent Examiner, Art Unit 2815